REMARKS

In the Office Action, the Examiner noted that claims 1-24 are pending in the application. The Examiner additionally stated that claims 1-24 are rejected. By this amendment, claim 20 has been cancelled and claims 1, 3-5, 11, 13, 18, and 21 have been amended. Hence, claims 1-19 and 21-24 are pending in the application.

Applicant hereby requests further examination and reconsideration of the application, in view of the foregoing amendments.

IN THE DRAWINGS

The Examiner objected to the drawings, noting that Figures 1 and 2 should be designated by a legend such as --Prior Art--. In response, Applicant has amended Figures 1 and 2 to provide the suggested legend. Formal drawings are herewith transmitted to the Official Draftsman and a courtesy copy of Figures 1 and 2 is attached to this amendment for review by the Examiner. Accordingly, Applicant requests that the Examiner withdraw his objections to the drawings.

IN THE SPECIFICATION

The Examiner objected to the specification, noting that the title of the invention is not descriptive. In response, Applicant has amended the title to clearly indicate the invention to which the claims are directed. Applicant has also amended the specification to secure a substantial correspondence between the claims amended herein and the remainder of the specification. No new matter is presented. Furthermore, Applicant has checked the specification for the presence of minor errors and has found none, but offers further cooperation in correcting any that may come to the attention of the Examiner. Applicant therefore requests that the Examiner withdraw his objection to the specification.

IN THE CLAIMS

Rejections Under 35 U.S.C. §102(b)

The Examiner rejected claims 18-21, and 23-24 under 35 U.S.C. 102(b) as being clearly anticipated by Richter et al., U.S. Patent Number 5,481,684 (hereinafter, "Richter"). Applicant respectfully traverses the Examiner's rejections.

Prior to providing a claim-by-claim analysis, a brief overview of Richter vis-à-vis is provided below to aid the Examiner during reconsideration.

Richter provides a mechanism for triggering a switch from a code segment containing CISC code to a code segment containing RISC code to allow for execution of CISC programs on a processor that emulates a CISC operating system using RISC code. The processor is capable of decoding both the RISC and CISC instruction sets. An undefined or reserved bit within a segment descriptor is used to indicate which instruction set the code in the segment is written in. The switch from CISC to RISC instruction set decoding is triggered when control is transferred to a new segment, and the segment descriptor indicates that the code within the segment is written in the alternate instruction set. (Abstract)

Applicant's invention, on the other hand, provides a mechanism in a pipeline microprocessor that enables programs written in native instructions to be executed directly from memory. The mechanism includes instruction translation logic and bypass logic. The instruction translation logic retrieves macro instructions provided via the external instruction bus, and decodes each of the macro instructions into associated native instructions for execution by the microprocessor. The instruction translation logic decodes a native bypass macro instruction into an unconditional jump native instruction directing that program control be transferred to a memory address containing the programmed native instructions. The bypass logic is coupled to the instruction translation logic. The bypass logic disables the instruction translation logic upon detection of the native bypass macro instruction, and provides the programmed native instructions for execution by the microprocessor, thereby bypassing the instruction translation logic.

Richter's invention limits operation of RISC and CISC code routines to separate code segments (col. 6, lines 27-28) and a switch to an alternate instruction set must be triggered by an event or execution of an instruction that requires the loading of a new segment register. The instant application for Applicant does not put forth any limitations that restrict macro instructions or native instructions to be provided in separate code segments. The unconditional jump native instruction, which is the result of translating a

native bypass macro instruction, is not restricted to branches that require loading of a new code segment descriptor.

The Examiner stated that Richter taught a microprocessor for execution micro instructions directly from memory, comprising:

a. Translation logic, for receiving macro instructions from the memory, and for decoding said macro instructions into corresponding micro instructions for execution by the microprocessor;

b. Mode detection logic, coupled to said translation logic, for detecting bypass macro instructions, and for directing the microprocessor to execute the micro instructions directly from memory rather than via said translation logic, said bypass macro instructions comprising:

i. A native branch macro instruction, directing that program control be transferred to a target address; and

ii. A native branch return macro instruction, directing that program control be transferred to a return address; and

iii. An instruction router, coupled to said mode detection logic, for receiving the micro instructions, and for routing the micro instructions to execution logic, thereby bypassing said translation logic.

Claim 18 is provided below for review.

18. (Currently amended): A microprocessor for executing micro instructions directly from memory, the microprocessor comprising:

translation logic, for receiving macro instructions from the memory, and for decoding said macro instructions into corresponding micro instructions for execution by the microprocessor;

mode detection logic, coupled to said translation logic, for detecting bypass macro instructions, and for directing the microprocessor to execute the micro instructions directly from the memory rather than via said translation logic, said bypass macro instructions comprising:

a native branch macro instruction, directing that program control be transferred to a target address, wherein said translation logic decodes said native branch macro instruction into an unconditional jump native instruction directing that program control be transferred to said target address, and wherein said target address contains the micro instructions; and

a native branch return macro instruction, directing that program control be transferred to a return address; and

an instruction router, coupled to said mode detection logic, for receiving the micro instructions, and for routing the micro instructions to execution logic, thereby bypassing said translation logic.

Applicant respectfully notes that the present invention includes native branch macro instruction, directing that program control be transferred to a target address. In addition, translation logic decodes the native branch macro instruction into an unconditional jump native instruction directing that program control be transferred to the target address, where the target address contains the micro instructions. Applicant has studied Richter and finds that he does not teach translation of a native branch macro instruction into an unconditional jump native instruction directing that program control be transferred to a target address. In fact, Richter speaks of an indicating mechanism within a segment descriptor that provides for CISC and RISC code to be executed by a processor, but the CISC and RISC code must reside in different segments. In view of these reasons, Applicant believes claim 18 to be allowable over Richter, and respectfully requests withdrawal of the rejection.

With respect to claims 19, 21, and 23-24, these claims depend from claim 18 and add further limitations that are neither anticipated nor made obvious by Richter. Accordingly, Applicant respectfully requests that the Examiner withdraw the rejections to claims 19, 21, and 23-24.

By this amendment, claim 20 has been cancelled, thereby rendering the Examiner's rejections moot.

Rejections Under 35 U.S.C. §103(a)

The Examiner rejected claims 1-17, and 22 under 35 U.S.C. 103(a) as being unpatentable over Richter, in view of Blomgren et al., U.S. Patent Number 5,781,750 (hereinafter, "Blomgren"). Applicant respectfully traverses the Examiner's rejections.

The Examiner noted with reference to claim 1 that Richter taught an apparatus in a microprocessor for executing programmed native instructions that are provided directly to the microprocessor, comprising:

a) Instruction translation logic, configured to retrieve macro instructions and configured to decode each of said macro instructions into associated native instructions for execution by the microprocessor; and

b) Bypass logic, coupled to said translation logic, configured to disable said instruction translation logic, and configured to provide the programmed native instructions for execution by the microprocessor, thereby bypassing said instruction translation logic.

The Examiner also stated that Richter has not explicitly taught an external instruction bus, but that Blomgren taught an external instruction bus.

In response, Applicant notes that, like claim 18, claim 1 recites a limitation "wherein said instruction translation logic decodes a native bypass macro instruction into an unconditional jump native instruction directing that program control be transferred to a memory address containing the programmed native instructions." This limitation is not alluded to in Richter, nor does Richter teach any other means for triggering a switch from CISC to RISC other than through setting a bit in a segment descriptor and then executing a far call instruction to access the descriptor. In addition, Blomgren does not suggest such a limitation either.

For these reasons, Applicant respectfully requests that the Examiner withdraw the rejection of claim 1.

Claims 2-10 depend from claim 1, and add further limitations which are neither anticipated nor made obvious by Richter, Blomgren, or Richter and Blomgren in

combination. Accordingly, it is respectfully requested that the rejections of claims 2-10 be withdrawn.

With regard to the rejection of claim 11, the Examiner made arguments substantially similar to those made in the rejection of claim 1. And like claim 1, the amendments to claim 11 recite a limitation that "said translator translates a native bypass macro instruction into an unconditional jump native instruction directing that program control be transferred to a memory address containing the micro instruction." In that neither Richter nor Blomgren teach such a mechanism as noted above, Applicant respectfully requests that the rejection of claim 11 be withdrawn.

Claims 12-17 depend from claim 11, and add further limitations which are neither anticipated nor made obvious by Richter, Blomgren, or Richter and Blomgren in combination. Accordingly, it is respectfully requested that the rejections of claims 12-17 be withdrawn.

In view of the arguments advanced above, Applicant respectfully submits that claims 1-19 and 21-24 are in condition for allowance. Reconsideration of the rejections is requested, and allowance of the claims is solicited.

Applicant earnestly requests that the Examiner contact the undersigned practitioner by telephone if the Examiner has any questions or suggestions concerning this amendment, the application, or allowance of any claims thereof.

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I hereby certify that this paper is being deposited with the U.S. Postal Service Express Mail Post Office to Addressee Service under 37 C.F.R. §1.10 on the date shown above and is addressed to Mail Stop PETITION, Commissioner for Patents, PO Box 1450, Alexandria, VA 22313-1450.

Respectfully submitted,

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